IN THE UNITED STATES PATENT AND TRADEMARK OFFICE

In re Application of: **Xiang, et al.**	Art Unit: 2815
Serial No.: 10/643,461	Examiner: Nguyen, Joseph H.
Filed: August 18, 2003	
For: **Field Effect Transistor Having Increased Carrier Mobility**	

APPEAL BRIEF

Mail Stop Appeal Brief - Patents
Honorable Commissioner for Patents
P.O. Box 1450
Alexandria, VA 22313-1450

Dear Sir/Madam:

This is an Appeal from the Examiner's Final Rejection of claims 1-3, 6-7, 9-10, 13, 15-16, and 19. The Final Rejection issued on March 3, 2005. The Notice of Appeal was filed in the U.S. Patent and Trademark Office on June 2, 2005.

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REAL PARTY IN INTEREST

The real party in interest is Advanced Micro Devices, Inc.

RELATED APPEALS AND INTERFERENCES

There are no related Appeals or Interferences.

STATUS OF CLAIMS

Claims 1-3, 6-7, 9-10, 13, 15-16, and 19 are pending, and claims 4-5, 8, 11-12, 14, 17-18, and 20 were canceled in previous amendments. Claims 1-3, 6-7, 9-10, 13, 15-16, and 19 have been finally rejected in a Final Rejection dated March 3, 2005. This Appeal is directed to the rejection of claims 1-3, 6-7, 9-10, 13, 15-16, and 19. Claims 1-3, 6-7, 9-10, 13, 15-16, and 19 appear in an Appendix to this Appeal Brief.

STATUS OF AMENDMENTS

No claim amendments have been submitted in response to or subsequent to the Final Rejection dated March 3, 2005.

SUMMARY OF CLAIMED SUBJECT MATTER

A. Claim 1

Independent claim 1 is directed to increased carrier mobility in a field effect transistor ("FET"), e.g. FET 102 in Figure 1, fabricated on a substrate, e.g. substrate 104

in Figure 1. More particularly, the claim is about increased carrier mobility in the channel of the FET, e.g. in channel 112 of FET 102 in Figure 1. Figure 1 shows a cross-sectional view of an exemplary FET in accordance with one embodiment of the present invention. FET 102 includes gate stack 106, which includes gate electrode 114 and gate dielectric 116, source 108, drain 110, and channel 112. *See, e.g., page 6 of the present application, lines 13-17.*

In one embodiment, gate electrode 114 and gate dielectric 116 are selected such that gate electrode 114 has a coefficient of thermal expansion ("CTE") that is higher than a CTE of gate dielectric 116. Thus, as a wafer comprising FET 102 cools down after gate electrode 114 has been deposited at high temperature, gate electrode 114 decreases in size to a greater extent (i.e. shrinks more) than gate dielectric 116. As a result, tensile strain is created in channel 112, which increases carrier mobility in FET 102. *See, e.g., page 7 of the present application, lines 7-13.*

In another embodiment, gate dielectric 116 and gate electrode 114 are selected such that gate dielectric 116 has a CTE that is higher than a CTE of gate electrode 114. In such embodiment, compressive strain is created in channel 112, which increases carrier mobility in FET 102. *See, e.g., page 7 of the present application, lines 13-17.* Thus, as claimed in claim1, gate dielectric 116 and gate electrode 114 are selected such that the difference between their respective coefficients of thermal expansion causes either a tensile strain or a compressive strain, thereby resulting in an increase in carrier mobility in FET 102.

B. Claim 9

Independent claim 9 is also directed to increased carrier mobility in a field effect transistor ("FET"), e.g. FET 102 in Figure 1. More particularly, the claim is about increased carrier mobility in the channel of the FET, e.g. in channel 112 of FET 102 in Figure 1. According to claim 9, and similar to claim 1, gate dielectric 116 and gate electrode 114 are selected such that the difference between their respective coefficients of thermal expansion causes either a tensile strain or a compressive strain, thereby resulting in an increase in carrier mobility in FET 102.

C. Claim 15

Similar to claims 1 and 9, independent claim 15 is directed to increased carrier mobility in a FET channel, e.g. channel 112 of FET 102 in Figure 1. In contrast to claims 1 and 9, claim 15 expressly recites a channel and expresses that the strain caused in the channel is a result of different coefficients of thermal expansion of the gate electrode and the gate dielectric. Claim 15 also expressly recites that gate electrode 114 and gate dielectric 116 are part of a "gate stack," i.e. gate stack 106 in Figure 1.

Thus, similar to claims 1 and 9, gate dielectric 116 and gate electrode 114 are selected such that the difference between their respective coefficients of thermal expansion causes either a tensile strain or a compressive strain, thereby resulting in an

increase in carrier mobility in FET 102. *See, e.g., page 7 of the present application, lines 7-17.*

GROUNDS OF REJECTION TO BE REVIEWED ON APPEAL

A. Claims 1-3, 6, 9-10, and 15-16 stand rejected under 35 U.S.C. §102(b) as being anticipated by U.S. Patent No. 6,190,975 to Kubo, et al (hereinafter "Kubo").

B. Claims 7, 13, and 19 stand rejected under 35 U.S.C. §103 as being unpatentable over Kubo.

ARGUMENT

A. Rejection of claims 1-3, 6, 9-10, and 15-16 under 35 U.S.C. §102(b) as being anticipated by Kubo

The Examiner has rejected claims 1-3, 6, 9-10, and 15-16 under 35 USC §102(b) as being anticipated by U.S. patent number 6,190,975 to Kubo et al ("Kubo"). For the reasons discussed below, Applicants submit that the present invention, as defined by independent claims 1, 9, and 15, is patentably distinguishable over Kubo.

At the outset, Applicants submit that Kubo is in fact an improper anticipation reference for the present invention. If the Examiner had cited an appropriate anticipation art reference, the issues in this appeal could be more appropriately addressed. The Examiner has implicitly acknowledged that Kubo is not an anticipation art reference by citing two pages from "Silicon Processing for the VLSI Era" by Wolf et al (hereinafter "Wolf") (it is noted that the Examiner cited this reference for the first time in the final

rejection). The Examiner has utilized Wolf to overcome the glaring deficiency in Kubo, in that, as stated below, Kubo does not even mention a coefficient of thermal expansion.

The present invention, as defined by amended independent claims 1, 9, and 15 includes, among other things, a first gate dielectric having a first coefficient of thermal expansion and a first gate electrode having a second coefficient of thermal expansion, where "said first gate dielectric and said first gate electrode are selected such that a difference between said second coefficient of thermal expansion and said first coefficient of thermal expansion causes an increase in carrier mobility in said FET." As disclosed in the present application, the FET includes a gate electrode layer situated over a gate dielectric layer, where the gate electrode layer and the gate dielectric layer are selected such that the gate electrode layer has a coefficient of thermal expansion ("CTE") that is higher than a CTE of the gate dielectric layer. As disclosed in the present application, as a wafer comprising the gate electrode and gate dielectric layers cools down after the gate electrode layer has been deposited at high temperature, the gate electrode layer decreases in size to a greater extent (i.e. shrinks more) than the gate dielectric layer. As further disclosed in the present application, as a result, tensile strain is created in a channel situated underneath the gate dielectric, which advantageously increases carrier mobility in the FET.

In one embodiment, the gate dielectric and gate electrode layers are selected such that the gate dielectric layer has a CTE that is higher than the CTE of the gate electrode layer. In such embodiment, compressive strain is created in the channel underneath the

gate dielectric layer, which increases carrier mobility in the FET. Thus, by selecting gate electrode and gate dielectric layers of a gate stack to have appropriate respective coefficients of thermal expansion, the present invention achieves increased tensile strain in the channel of a FET. As a result, the present invention advantageously achieves increased carrier mobility in the FET, which results in increased FET performance.

In contrast, Kubo does not teach, disclose, or even suggest a first gate dielectric having a first coefficient of thermal expansion and a first gate electrode having a second coefficient of thermal expansion, where "said first gate dielectric and said first gate electrode are selected such that a difference between said second coefficient of thermal expansion and said first coefficient of thermal expansion causes an increase in carrier mobility in said FET." Kubo discloses an NMOS transistor including SiGeC layer 14n, gate insulating layer 19n, and gate electrode 18n, where gate electrode 18n is situated over gate insulating layer 19n and gate insulating layer 19n is situated over SiGeC layer 14n, which serves as channel. See, for example, column 9, lines 7-23 and Figure 1 of Kubo. In Kubo, the composition rates of the respective elements in SiGeC layer 14n are set such that SiGeC layer 14n and Si layer 13n immediately therebelow "are fitted in lattice for each other." See, for example, column 8, lines 57-61 and Figure 1 of Kubo. According to Kubo, the fitted lattice prevents a defect, such as dislocation, from being induced in the SiGeC layer 14n channel. That is, if the SiGeC layer 14n and the Si layer 13n therebelow are "misfitted in lattice for each other," the SiGeC layer 14n is prone to have a defect impeding electron flow. Thus, Kubo merely discloses a SiGeC layer with

fewer defects; Kubo does not even address tensile or compressive strain caused by any reason, nor by the reason of a gate electrode and a gate dielectric having different CTEs.

Further, according to Kubo, SiGeC layer 14n has a higher electron mobility than Si layer 13n, thus increasing the operational speed of the NMOS transistor. See, for example, Kubo, column 9, lines 4-6. However, as stated above, Kubo fails to teach, disclose, or even suggest a first gate dielectric and a first gate electrode being selected such that a difference between the second coefficient of thermal expansion of the first gate electrode and the first coefficient of thermal expansion of the first gate dielectric causes an increase in carrier mobility in the FET. Indeed, Kubo fails to even mention a coefficient of thermal expansion.

As stated above, Kubo is in fact an improper anticipation reference for the present invention. If the Examiner had cited an appropriate anticipation art reference, the issues could be more appropriately addressed. The Examiner has implicitly acknowledged that Kubo is not an anticipation art reference, by citing two pages from "Silicon Processing for the VLSI Era" by Wolf et al (hereinafter "Wolf"). The Examiner has utilized Wolf to overcome the glaring deficiency in Kubo, in that, as stated above, Kubo does not even mention a coefficient of thermal expansion. The Examiner has essentially argued that Wolf discloses that the CTE is an inherent characteristic of any give layer, and different CTEs would result in the present invention. First, reliance on Wolf makes the Examiner's anticipation reference improper; and the anticipation rejection should thus be reversed. Second, the Examiner has suggested (without even Wolf suggesting so), that "silicon" can

be used as an electrode since silicon has a CTE different than the CTE of silicon oxide. However, Wolf lists "silicon" as having a sheet resistance of 230 Kilo Ohms-Centimeter (Appendix 1 relied upon by the Examiner). As such, silicon cannot be used as an electrode due to extremely high resistance. The Examiner has used the word "polysilicon" for use as an electrode, but there is no reference in Wolf for using polysilicon as an electrode or any discussion of what the CTE of polysilicon is; Wolf only refers to silicon and not polysilicon.

For the foregoing reasons, Applicants respectfully submit that the present invention, as defined by independent claims 1, 9, and 15, is not taught, disclosed, or even suggested by Kubo. Thus, independent claims 1, 9, and 15 are patentably distinguishable over Kubo. As such, the claims 2-3, 6, 10, and 16 depending from independent claims 1, 9, and 15 are, *a fortiori*, also patentably distinguishable over Kubo for at least the reasons presented above and also for additional limitations contained in each dependent claim. At a minimum, for the reasons mentioned above, Kubo does not anticipate the claimed invention now before the Board.

B. Rejection of claims 7, 13, and 19 under 35 U.S.C. §103 as being unpatentable over Kubo

The Examiner has rejected claims 7, 13, and 19 under 35 USC §103(a) as being unpatentable over Kubo. However, as discussed above, independent claims 1, 9, and 15 are patentably distinguishable over Kubo. Thus, claim 7 depending from independent claim 1; claim 13 depending from independent claim 9, and claim 19 depending from

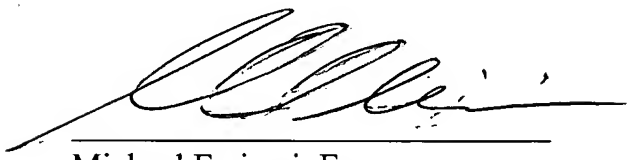
independent claim 15 are, *a fortiori*, also patentably distinguishable over Kubo for at least the reasons presented above and also for additional limitations contained in each dependent claim. At a minimum, for the reasons mentioned above, Kubo does not anticipate the claimed invention now before the Board.

CONCLUSION

Based on the foregoing reasons, the present invention, as defined by independent claims 1, 9, and 15, and claims depending therefrom, is patentably distinguishable over the art cited by the Examiner. At a minimum, for the reasons mentioned above, Kubo does not anticipate the invention claimed by independent claims 1, 9, and 15. As such, and for all the foregoing reasons, an early allowance of claims 1-3, 6-7, 9-10, 13, 15-16, and 19 pending in the present application is respectfully requested.

This Appeal Brief is submitted herewith with an Appendix of the appealed claims and the requisite fee for filing the Appeal Brief.

Respectfully Submitted,
FARJAMI & FARJAMI LLP



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Date: 7/25/05

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CERTIFICATE OF MAILING

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Date of Deposit: 7/25/05

Christina Carter
Name of Person Mailing Paper and/or Fee

Christina Carter 7/25/05
Signature Date

APPENDIX OF CLAIMS ON APPEAL

Claim 1: A FET situated over a substrate, said FET comprising:

a channel situated in said substrate;

a first gate dielectric situated over said channel, said first gate dielectric having a first coefficient of thermal expansion;

a first gate electrode situated over said first gate dielectric, said first gate electrode having a second coefficient of thermal expansion;

wherein said first gate dielectric and said first gate electrode are selected such that a difference between said second coefficient of thermal expansion and said first coefficient of thermal expansion causes an increase in carrier mobility in said FET.

Claim 2: The FET of claim 1 wherein said second coefficient of thermal expansion is greater than said first coefficient of thermal expansion.

Claim 3: The FET of claim 2 wherein said increase in said carrier mobility is caused by a tensile strain created in said channel.

Claim 6: The FET of claim 1 wherein said FET is a PFET.

Claim 7: The FET of claim 6 wherein said first coefficient of thermal expansion is greater than said second coefficient of thermal expansion so as to cause a compressive

strain in said channel, said compressive strain causing said increase in said carrier mobility.

Claim 9: A FET situated over a substrate, said FET comprising a channel situated in said substrate, a first gate dielectric situated over said channel, said first gate dielectric having a first coefficient of thermal expansion, a first gate electrode situated over said first gate dielectric, said first gate electrode having a second coefficient of thermal expansion, said FET being characterized in that:

said first gate dielectric and said first gate electrode are selected such that a difference between said second coefficient of thermal expansion and said first coefficient of thermal expansion causes an increase in carrier mobility in said FET.

Claim 10: The FET of claim 9 wherein said second coefficient of thermal expansion is greater than said first coefficient of thermal expansion so as to cause a tensile strain in said channel, said tensile strain causing said increase in said carrier mobility.

Claim 13: The FET of claim 9 wherein said FET is a PFET, said first coefficient of thermal expansion being greater than said second coefficient of thermal expansion so as to cause a compressive strain in said channel, said compressive strain causing said increase in said carrier mobility.

Claim 15: A FET situated on a substrate, said FET comprising:

a channel situated in said substrate;

a gate stack situated over said channel;

a first gate dielectric situated in said gate stack, said first gate dielectric having a first coefficient of thermal expansion;

a first gate electrode situated over said first gate dielectric, said first gate electrode having a second coefficient of thermal expansion;

wherein said first gate dielectric and said first gate electrode are selected such that a difference between said second coefficient of thermal expansion and said first coefficient of thermal expansion causes a strain in said channel, said strain causing an increase in carrier mobility in said FET.

Claim 16: The FET of claim 15 wherein said second coefficient of thermal expansion is greater than said first coefficient of thermal expansion so as to cause a tensile strain in said channel, said tensile strain causing said increase in said carrier mobility.

Claim 19: The FET of claim 15 wherein said FET is a PFET, said first coefficient of thermal expansion being greater than said second coefficient of thermal expansion so

as to cause a compressive strain in said channel, said compressive strain causing said increase in said carrier mobility.

PTO/SB/17 (12-04)
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U.S. Patent and Trademark Office: U.S. DEPARTMENT OF COMMERCE

Effective on 12/8/2004.
Fees pursuant to the Consolidated Appropriations Act, 2005 (H.R. 4818).

FEE TRANSMITTAL
For FY 2005

		Complete if Known	
		Application Number	10/643,461
		Filing Date	08/18/2003
		First Named Inventor	Xiang
		Examiner Name	Nguyen, Joseph H.
☐ Applicant Claims small entity status. See 37 CFR 1.27		Art Unit	2815
TOTAL AMOUNT OF PAYMENT	$500.00	Attorney Docket No.	0180144

METHOD OF PAYMENT (check all that apply)

☐ Check ☒ Credit Card ☐ Money Order ☐ None ☐ Other (please identify): _____

☒ Deposit Account Deposit Account Number: **50-0731** Deposit Account Name: **Farjami & Farjami LLP**

For the above-identified deposit account, the Director is hereby authorized to: (check all that apply)

☐ Charge fee(s) indicated below ☐ Charges fee(s) indicated below, **except for the filing fee**

☒ Charge any additional fee(s) or underpayments of fee(s) under 37 CFR 1.16 and 1.17 ☒ Credit any overpayments

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FEE CALCULATION

1. BASIC FILING, SEARCH, AND EXAMINATION FEES

	FILING FEES	Small Entity	SEARCH FEES	Small Entity	EXAMINATION FEES	Small Entity	
Application Type	Fee ($)	Fee ($)	Fee ($)	Fee ($)	Fee ($)	Fee ($)	Fees Paid ($)
Utility	300	150	500	250	200	100	
Design	200	100	100	50	130	65	
Plant	200	100	300	150	160	80	
Reissue	300	150	500	250	600	300	
Provisional	200	100	0	0	0	0	

2. EXCESS CLAIM FEES

Fee Description	Fee ($)	Small Entity Fee ($)
Each claim over 20 or, for Reissues, each claim over 20 and more than in the original patent	50	25
Each independent claim over 3 or, for Reissues, each independent claim more than in the original patent	200	100
Multiple dependent claims	360	180

Total Claims		Extra Claims		Fee ($)		Fee Paid ($)
_____	- 20 or HP =	0	x	$50.00	=	$ 0.00

HP = highest number of total claims paid for, if greater than 20

Indep. Claims		Extra Claims		Fee ($)		Fee Paid ($)
_____	- 3 or HP =	0	x	$200.00	=	$ 0.00

HP = highest number of independent claims paid for, if greater than 3

Multiple Dependent Claims Fee ($)	Fee Paid ($)
$360.00	

3. APPLICATION SIZE FEE

If the specification and drawings exceed 100 sheets of paper, the application size fee due is $250 ($125 for small entity) for each additional 50 sheets or fraction thereof. See 35 U.S.C. 41 (a)(1)(G) and 37 CFR 1.16(s).

Total Sheets		Extra Sheets		Number of each additional 50 or fraction thereof		Fee ($)		Fee Paid ($)
_____	- 100 =	0	/ 50 =	0	(round up to a whole number) x	$250.00	=	$ 0.00

4. OTHER FEE(S) Fees Paid($)

Non-English Specification, $130 fee (no small entity discount) _____

Other: **Filing a brief in support of an appeal** **$500.00**

SUBMITTED BY

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Name (Print/Type)	Michael Farjami, Esq.		Date 7/25/05